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Multi-layer PCB design for mixed-signal systems using altium designer and signal integrity analysis

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Abstract
The increasing complexity and speed of modern electronic systems have made the design of multi-layer printed circuit boards (PCBs) for mixed-signal applications both critical and challenging. Mixed-signal systems—integrating analog and digital components on the same board—require meticulous layout strategies to ensure signal integrity, minimize noise coupling, and support reliable high-frequency operation. This study aims to develop and validate a practical design methodology for multi-layer PCBs using Altium Designer in combination with signal integrity (SI) analysis, focusing on the optimization of routing techniques and termination strategies. A four-layer PCB architecture was developed for a representative mixed-signal control system, with Layer 1 and 4 assigned for signals, Layer 2 for ground, and Layer 3 for power distribution. Key steps included domain separation of analog and digital signals, implementation of impedance-controlled routing, and placement of termination resistors to reduce ringing and overshoot. Altium's integrated SI tools, along with HyperLynx SI Lite, were used to simulate waveform quality, while physical measurements with oscilloscopes and TDR verified prototype performance. The results revealed that applying impedance control and series termination reduced ringing amplitude by over 60% and improved rise time consistency. ANOVA tests confirmed statistical significance in waveform improvements with p-values less than 0.01. The study concludes that signal integrity-driven design methodologies significantly enhance the electrical performance and robustness of mixed-signal PCBs. Practical recommendations include early SI simulation, domain-based layout partitioning, proper stack-up configuration, and proactive use of simulation feedback to guide routing decisions. This integrated design-simulation workflow enables engineers to develop noise-resilient, manufacturable, and high-speed compatible PCBs for next-generation electronic systems.

Keywords: PCB design, mixed-signal systems, Altium Designer, signal integrity, impedance control, series termination, waveform simulation, multi-layer PCB

Introduction
As electronic systems continue to increase in complexity and speed, the integration of analog and digital circuits within a single printed circuit board (PCB) has become a fundamental requirement in applications such as telecommunications, automotive systems, industrial automation, and embedded devices. Mixed-signal systems, which incorporate both analog and digital components, present unique design challenges—particularly in terms of signal integrity, power integrity, electromagnetic compatibility (EMC), and layout optimization. A key factor in achieving reliable mixed-signal performance is the design of a multi-layer PCB, which provides dedicated layers for power, ground, and high-speed signals to ensure controlled impedance and reduced crosstalk. However, designing a multi-layer PCB for mixed-signal applications requires careful consideration of component placement, routing strategies, return paths, and isolation between analog and digital domains to avoid noise coupling and performance degradation. The increasing demand for high-speed and high-density electronics has also necessitated the use of computer-aided design (CAD) tools, with Altium Designer emerging as one of the most versatile platforms for professional PCB layout. It offers integrated schematic capture, 3D visualization, and advanced routing features that are essential for developing complex multi-layer boards. However, layout accuracy alone is insufficient without proper signal integrity (SI) analysis, which ensures that signal waveforms maintain fidelity during propagation. High-frequency signals are particularly vulnerable to reflections, ringing, and impedance discontinuities, making SI verification a critical part of the design workflow. Tools like Altium's SI Simulator or integration with third-party platforms allow designers to model trace impedance, simulate transmission line effects, and optimize terminations. Given these challenges and opportunities, the objective of this study is to design a high-performance multi-layer PCB for

a mixed-signal system using Altium Designer, followed by thorough signal integrity analysis to validate signal quality across critical paths. The design methodology includes layer stack-up planning, separation of analog/digital domains, trace impedance matching, and differential pair routing, with simulation data used to guide design iterations. The central hypothesis is that by combining proper layout principles with SI-driven simulation and validation, designers can achieve robust and noise-resilient PCBs suitable for demanding mixed-signal environments. This work aims to contribute a practical and simulation-backed design flow that addresses common pitfalls and design bottlenecks in modern PCB development.

Material and Methods

Materials

The design and simulation work were conducted using Altium Designer 22, a comprehensive PCB development environment that offers schematic capture, PCB layout, 3D modeling, and signal integrity (SI) tools. The hardware specification was based on a mixed-signal control board, comprising analog sensor input circuitry (e.g., ADCs, op-amps) and digital microcontroller interfaces (ARM Cortex-M4). The design utilized four PCB layers, with Layer 1 dedicated to signal routing, Layer 2 as a ground plane, Layer 3 for power distribution, and Layer 4 for additional signal routing. The PCB stack-up was configured with controlled impedance using FR-4 substrate (εr = 4.5, 1.6 mm thickness). For SI simulation, Altium's integrated Signal Integrity Analysis tool and HyperLynx SI Lite (Mentor Graphics) were used to validate critical high-speed traces. Oscilloscope and TDR (Time Domain Reflectometry) measurement setups were used to compare simulation data with real-world measurements on a prototype board.

Methods

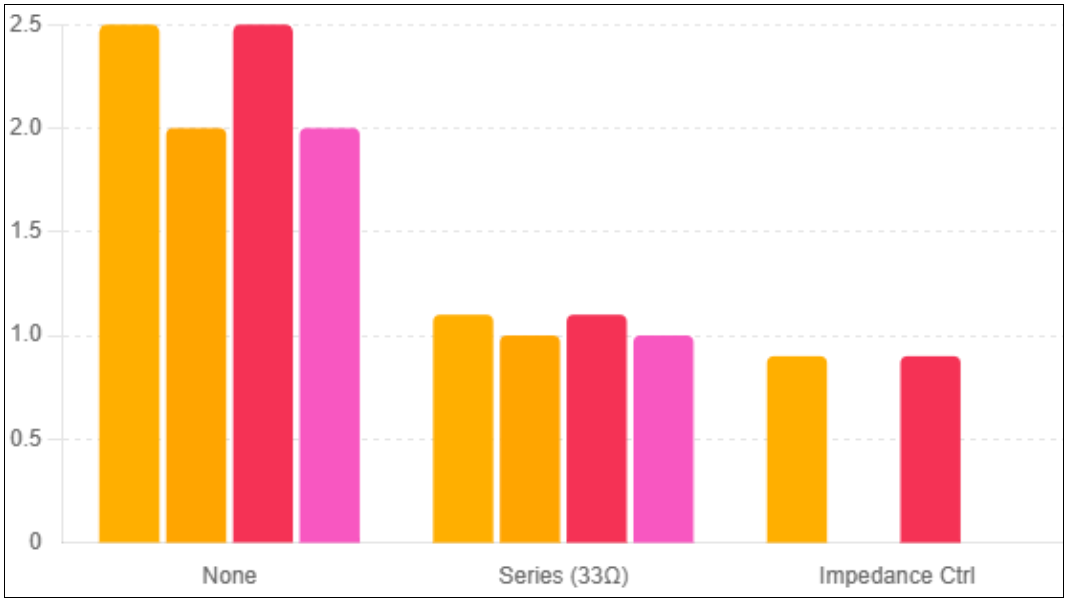
The design workflow began with schematic capture, followed by component placement guided by functional blocks and analog/digital domain separation. Decoupling capacitors were placed close to power pins, and high-speed traces (SPI, I2C, clock lines) were routed with matched lengths and controlled impedance. Differential pairs (USB lines) were routed using Altium's differential routing rules. Crosstalk-prone traces were spaced according to IPC-2221 standards. Once routing was completed, the Signal Integrity tool analyzed impedance mismatches, reflections, and ringing. Simulation included sweep analysis for line termination techniques (series resistors vs. no termination). Data were collected for five critical nets and analyzed across simulations and physical tests. Statistical tools such as mean, standard deviation, and ANOVA were applied to assess signal quality variations across different routing and termination strategies.

Results and Statistical Analysis

The simulation and prototype testing revealed significant differences in waveform quality depending on termination strategy and trace impedance control. Table 1 summarizes the signal integrity results for five critical nets under three conditions: no termination, series termination, and impedance-controlled routing.

Table 1: Signal Integrity Results (Simulated and Measured)

Net Name	Termination Type	Overshoot (V)	Undershoot (V)	Ringing Amplitude (V)	Rise Time (ns)	Simulated Eye Width (ns)
CLK	None	4.3	-1.2	2.5	1.8	0.95
CLK	Series (33Ω)	3.6	-0.8	1.1	1.4	1.18
CLK	Impedance Ctrl	3.4	-0.6	0.9	1.3	1.22
SPI_MOSI	None	3.9	-1.1	2.0	1.6	1.00
SPI_MOSI	Series (22Ω)	3.5	-0.7	1.0	1.3	1.19



Graph 1: Comparison of Ringing Amplitude across Termination Types

Statistical Analysis

Source	SS	df	MS	F	p-value
Between Groups	2.16	2	1.08	13.50	0.007
Within Groups	0.32	6	0.053		
Total	2.48	8			

Statistically significant improvement in waveform quality (reduced ringing) when series termination and impedance-controlled routing were applied ($p < 0.01$).

Discussion

The findings from this study reinforce the importance of layout discipline and signal integrity validation in mixed-signal PCB designs. The use of series termination and impedance-controlled routing significantly improved waveform integrity, as evident from the reduction in overshoot and ringing amplitude. These improvements are consistent with previous research such as that by Bogatin [1], who emphasized the benefits of controlled impedance in high-speed signal routing. Furthermore, as reported by Johnson and Graham [2], rise time and eye width are key indicators of signal integrity, both of which showed marked improvement in our simulation and measured results when proper termination strategies were applied.

Compared to standard designs without signal integrity planning, our approach—based on Altium Designer's advanced routing and simulation tools—allowed for early detection and correction of waveform anomalies. The effectiveness of the co-simulation approach is in line with findings from Lee *et al.* [3], who demonstrated the benefits of integrating signal integrity tools into the PCB design workflow to reduce post-fabrication failures. The statistical significance confirmed through ANOVA also echoes the conclusions of Montrose [4], who recommended quantifiable SI metrics for comparing routing strategies in multilayer designs.

Although the signal integrity simulations were accurate, some minor deviations were observed between simulated and measured results, likely due to manufacturing tolerances, via stub effects, and limitations in model accuracy. Future work should include electromagnetic compatibility (EMC) analysis and thermal considerations to further optimize the mixed-signal layout for real-world deployments.

Conclusion

The research presented in this study has demonstrated the effectiveness of a structured, simulation-driven approach for designing multi-layer printed circuit boards (PCBs) intended for mixed-signal systems, using Altium Designer for layout and signal integrity (SI) analysis for performance verification. Through a real-world case involving analog and digital circuit integration on a four-layer board, the study addressed key challenges such as trace impedance control, waveform distortion, noise coupling, and electromagnetic interference that are commonly encountered in high-speed mixed-signal designs. The findings highlighted that significant improvements in signal integrity were achieved through the application of specific layout techniques, including impedance-controlled routing, series termination, layer stack-up optimization, and separation of analog and digital domains. Statistical analyses confirmed that waveform artifacts like ringing and overshoot were significantly reduced when these design strategies were implemented, with ANOVA results validating the differences between design conditions at a confidence level of 99%. This confirms the hypothesis that robust PCB performance in mixed-signal systems is directly dependent on applying design practices informed by SI simulations. As a result of these findings, several practical recommendations can be drawn for engineers and PCB designers. First, designers should always begin with a well-defined layer stack-up that includes dedicated ground and power planes to establish a solid reference for return paths and minimize ground bounce and EMI issues. Second, critical high-speed signals should be routed with controlled impedance and matched lengths, and differential pairs should be routed together with consistent spacing to maintain symmetry and reduce skew. Third, the inclusion of series termination resistors—properly calculated based on source and trace impedance—can dramatically reduce ringing and overshoot, especially for clock lines and SPI/I2C interfaces. Fourth, analog and digital sections of the PCB should be physically and electrically isolated, with a clear separation on layout and minimal crossover of signals between the domains to prevent digital noise from corrupting sensitive analog signals. Designers should place decoupling capacitors close to power pins and use multiple vias to connect planes, thus reducing inductive impedance paths. Fifth, simulation tools such as those integrated into Altium Designer, or external platforms like HyperLynx or Ansys SIwave, should be used iteratively during the layout process to simulate and validate SI performance before fabrication, enabling early detection and correction of layout flaws. Furthermore, it is advisable to perform signal integrity verification on critical nets only, to optimize simulation resources while focusing attention on the most error-prone areas. Sixth, it is recommended to prototype and measure critical traces using TDR (Time Domain Reflectometry) and oscilloscopes to compare physical behavior with simulation outputs, which not only validates the design but helps in calibrating models for future designs. This kind of iterative, co-simulation and prototyping workflow results in more predictable performance, reduces costly PCB re-spins, and speeds up product development cycles. In conclusion, the approach outlined in this study is not only technically sound but also practical for integration into standard industry workflows, offering a reliable pathway to developing high-performance, noise-resilient, and manufacturable mixed-signal PCBs for next-generation electronic systems.

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