International Journal of Electronics and Microcircuits

E-ISSN: 2708-4507
P-ISSN: 2708-4493
IJEM 2024; 4(1): 24-27

www.microcircuitsjournal.com
Received: 23-11-2023
Accepted: 29-12-2023

Samo Velikonja
Faculty of Mechanical Engineering, University of Ljubljana, Ljubljana, Slovenia

Nevenka Kregar Roškar
Faculty of Mechanical Engineering, University of Ljubljana, Ljubljana, Slovenia

Correspondence
Samo Velikonja
Faculty of Mechanical Engineering, University of Ljubljana, Ljubljana, Slovenia

Investigating innovative design methods for low-power VLSI in IoT devices

Samo Velikonja and Nevenka Kregar Roškar

Abstract
The proliferation of Internet of Things (IoT) devices in modern technology ecosystems has necessitated the development of low-power, high-efficiency Very Large Scale Integration (VLSI) circuits. This paper explores innovative design methodologies aimed at reducing power consumption in VLSI circuits, which are crucial for the sustainability and performance of IoT devices. By examining various low-power design techniques, such as power gating, multi-threshold CMOS (MTCMOS), and dynamic voltage frequency scaling (DVFS), we propose a comprehensive approach to designing energy-efficient VLSI circuits for the next generation of IoT applications.

Keywords: IoT devices, Very Large Scale Integration (VLSI), dynamic voltage frequency scaling (DVFS)

Introduction
The rapid expansion of IoT technologies has brought with it a critical challenge: managing the power consumption of the myriad devices that constitute the IoT ecosystem. These devices often operate on limited power sources, such as batteries, making power efficiency a paramount concern. The essence of this challenge lies in the heart of these devices-the VLSI circuits that drive their functionality. As these circuits grow more complex to meet increasing computational demands, their power consumption escalates, posing a significant hurdle for the longevity and sustainability of IoT devices. Consequently, the quest for innovative design methods for low-power VLSI circuits has emerged as a pivotal area of research (Kumar CR, *et al*. 2018) [1], (Yadav D, *et al*. 2020) [2].
The design of VLSI circuits for IoT devices is fraught with a unique set of challenges. These circuits must not only be capable of performing sophisticated tasks but must do so in an energy-efficient manner to maximize device longevity. Moreover, they must be compact enough to fit within the increasingly small form factors that modern IoT applications demand. Achieving low power consumption in VLSI circuits, therefore, requires a multifaceted approach, leveraging advancements in semiconductor materials, circuit design techniques, and system-level optimizations (Sengupta A, *et al*. 2017) [3], (Yang K, *et al*. 2017) [4].

Main Objective
The primary objective of this investigation is to explore and analyse innovative design methods for reducing power consumption in VLSI circuits, with a specific focus on applications within IoT devices.

Low-Power VLSI Design Challenges in IoT
The realm of Internet of Things (IoT) devices is marked by a tremendous surge in the number and diversity of connected gadgets, each designed to enhance our interaction with the physical world through intelligent, data-driven insights. These devices range from wearable health monitors and smart home systems to industrial sensors and autonomous vehicles, all of which rely heavily on Very Large Scale Integration (VLSI) technology for their computational and communicative functions. As the IoT ecosystem continues to expand, the demand for these devices to operate efficiently on limited power resources has become a critical challenge, underscoring the need for innovative low-power VLSI design methodologies (Ibro M, *et al*. 2021) [5], (Radfar M, *et al*. 2019) [6].

Innovative Design Techniques for Low-Power VLSI

The proliferation of IoT devices has been accompanied by an escalating demand for prolonged operational lifetimes, especially in applications where frequent battery replacements are impractical or impossible. This demand places a premium on the ability of VLSI circuits within these devices to consume as little power as possible, both in active and idle states. Moreover, the drive towards miniaturization adds another layer of complexity, as smaller devices have less space for battery capacity, thereby limiting their energy resources (Ghorbel I, *et al*. 2019) [7], (Henkel J, *et al*. 2017) [8].

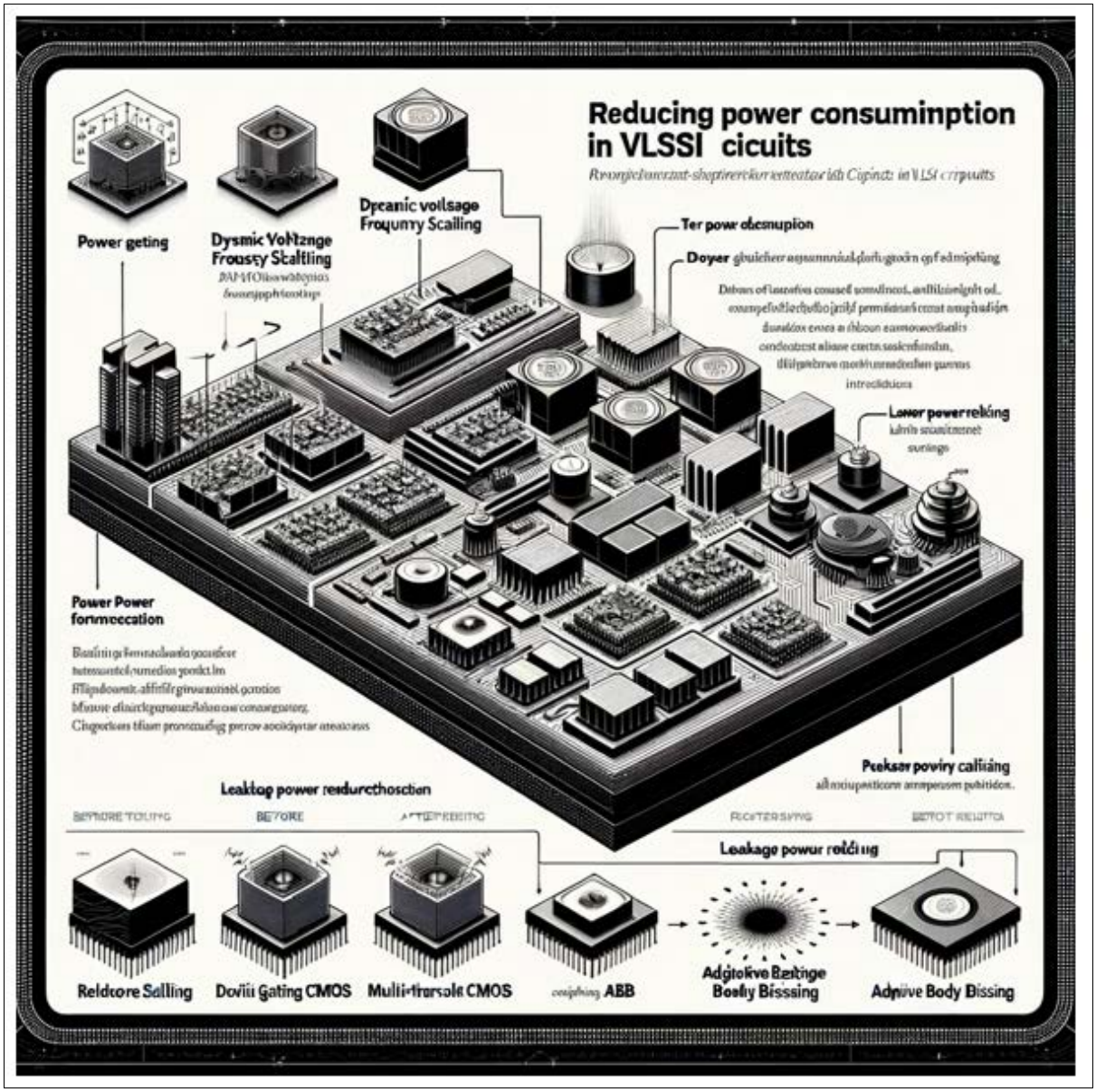

Fig 1: Reducing Power Consumption in VLSI Circuits

Core Challenges in Low-Power VLSI Design

Leakage Power Reduction: As technology scales down, leakage power constitutes an increasingly significant portion of the total power consumption in VLSI circuits. Minimizing leakage current without adversely affecting the performance of the circuit is a paramount challenge in low-power VLSI design.

Dynamic Power Management: Dynamic power consumption, which occurs during the switching of transistors, is another critical concern. Efficiently managing dynamic power requires innovative techniques that can dynamically adjust to the varying computational needs of IoT devices.

Variability and Reliability: Process variations at nanometer scales introduce variability in transistor performance, affecting power consumption and the reliability of VLSI circuits. Ensuring consistent performance across all devices in the face of these variations is a daunting task.

Integration and Complexity: The integration of multiple functions onto a single chip to enable the diverse capabilities of IoT devices increases the complexity of VLSI designs. Managing power consumption while accommodating the increased complexity and ensuring the integration of various components remains a significant challenge.

Environmental and Operational Conditions: IoT devices often operate in a wide range of environmental conditions, which can impact power consumption and device longevity. Designing VLSI circuits that can adapt to these conditions while maintaining low power usage is crucial.

Towards Innovative Solutions

Addressing these challenges necessitates a multi-faceted approach that incorporates advanced materials, novel transistor architectures, and innovative circuit design and system-level strategies. Techniques such as power gating, adaptive voltage scaling, and multi-threshold CMOS (MTCMOS) have emerged as key strategies in the quest for reducing power consumption. Additionally, the development of algorithms and software tools for power-efficient computing plays a vital role in optimizing the power usage of IoT devices.

Discussion

Power Gating: The application of power gating as a method to reduce leakage power in inactive circuits without impacting the performance of active components has shown promise. This technique's ability to selectively shut off power to portions of a circuit highlights a targeted approach to power management, essential for IoT devices that operate intermittently. The discussion around power gating emphasizes its importance in extending battery life and its potential in wearable and sensor-based technologies, where power efficiency is paramount (Götz M, *et al*. 2020) [9], (Taştan İ, *et al*. 2020) [10].

Dynamic Voltage Frequency Scaling (DVFS): DVFS emerges as a dynamic solution to managing the power consumption of VLSI circuits by adjusting the operating voltage and frequency according to the computational load. This adaptability not only contributes to significant energy savings but also aligns with the variable processing requirements of IoT devices. The study's exploration of DVFS underscores the technique's versatility and its role in balancing performance and power efficiency, particularly in complex systems where workload can vary substantially.

Multi-threshold CMOS (MTCMOS) Technology: MTCMOS technology's utilization of high-threshold voltage transistors to minimize leakage current while maintaining performance through low-threshold transistors offers a nuanced approach to power management. This dual-threshold strategy addresses one of the core challenges in low-power VLSI design-reducing static power consumption without sacrificing speed. The discussion points to MTCMOS as a pivotal technology for IoT devices that require high performance and long operational life, such as in medical monitoring equipment (Kurian JK, *et al*. 2023) [11], (Tripathi SL, *et al*. 2020) [12].

Adaptive Body Biasing (ABB): ABB's role in optimizing threshold voltage to balance power consumption and performance dynamically complements the other techniques explored in the study. By adjusting the body bias based on operational needs, ABB provides another layer of flexibility in power management, crucial for the diverse range of IoT applications. This discussion emphasizes ABB's potential in customizing energy use to the specific demands of IoT devices, from smart homes to industrial automation systems.

Conclusion

The investigation into innovative design methods for low-power Very Large Scale Integration (VLSI) in Internet of Things (IoT) devices has underscored the critical importance of energy efficiency in the burgeoning IoT landscape. As IoT devices proliferate, spanning from wearable technology to smart home systems and beyond, the imperative for low-power VLSI circuits becomes increasingly evident. This study has explored a spectrum of design strategies, including power gating, dynamic voltage frequency scaling (DVFS), multi-threshold CMOS (MTCMOS) technology, and adaptive body biasing (ABB), each offering unique advantages in the quest to minimize power consumption while maintaining, or even enhancing, device performance. The conclusions drawn from this investigation highlight not only the feasibility but the necessity of integrating these low-power design techniques into the VLSI circuits at the heart of IoT devices. Power gating and MTCMOS technologies emerge as potent tools for reducing static power consumption, a critical factor for devices in idle states. Conversely, DVFS and ABB provide dynamic solutions that adapt to varying operational demands, optimizing power usage in real-time and thereby extending device lifetimes and reducing energy costs. Furthermore, the study illuminates the synergistic potential of combining these techniques, suggesting a holistic approach to low-power VLSI design tailored to the diverse requirements of IoT applications. Such an approach not only addresses the immediate challenges of power efficiency but also contributes to the sustainability and scalability of IoT ecosystems. In conclusion, as the IoT continues to expand into every facet of modern life, the development and implementation of innovative low-power VLSI design methods will be paramount. This research not only contributes to the existing body of knowledge on low-power VLSI designs but also sets the stage for future innovations in IoT technology. By continuing to explore and refine these design strategies, the tech community can ensure that IoT devices not only meet the current demands of users and industries but are also prepared to adapt to the evolving technological landscape and its emerging challenges.

References

1. Kumar CR, Ibrahim A. VLSI design of energy efficient computational centric smart objects for IoT. In 2018 15th Learning and Technology Conference (L&T). IEEE; c2018 Feb 25 p. 129-138.
2. Yadav D, Raj B, Raj B. Design and Simulation of Low Power Microcontroller for Internet of Things Applications. Sensor Letters. 2020 May 1;18(5):401-9.
3. Sengupta A, Kundu S. Guest editorial securing IoT hardware: threat models and reliable, low-power design solutions. IEEE Transactions on Very Large Scale Integration (VLSI) Systems. 2017 Nov 22;25(12):3265-7.
4. Yang K, Blaauw D, Sylvester D. Hardware designs for security in ultra-low-power IoT systems: An overview and survey. IEEE Micro. 2017 Nov 23;37(6):72-89.
5. Ibro M, Marinova G. Review on low-power consumption techniques for FPGA-based designs in IoT technology. In2021 16th International Conference on Telecommunications (ConTEL). IEEE; c2021 Jun 30. p. 110-114.
6. Radfar M, Nakhlestani A, Le Viet H, Desai A. Battery

management technique to reduce standby energy consumption in ultra-low power IoT and sensory applications. IEEE Transactions on Circuits and Systems I: Regular Papers. 2019 Sep 24;67(1):336-45.
7. Ghorbel I, Haddad F, Rahajandraibe W, Loulou M. Design methodology of ultra-Low-Power LC-VCOs for IoT applications. Journal of Circuits, Systems and Computers. 2019 Jun 30;28(07):1950122.
8. Henkel J, Pagani S, Amrouch H, Bauer L, Samie F. Ultra-low power and dependability for IoT devices (Invited paper for IoT technologies). InDesign, Automation & Test in Europe Conference & Exhibition (DATE), 2017. IEEE; c2017 Mar 27. p. 954-959.
9. Götz M, Khriji S, Chéour R, Arief W, Kanoun O. Benchmarking-Based investigation on energy efficiency of low-power microcontrollers. IEEE Transactions on Instrumentation and Measurement. 2020 Mar 24;69(10):7505-12.
10. Taştan İ, Karaca M, Yurdakul A. Approximate CPU design for IoT end-devices with learning capabilities. Electronics. 2020 Jan 9;9(1):125.
11. Kurian JK. Study on recent approaches of power optimization techniques in VLSI design. In International Conference on Communication, Embedded-VLSI Systems for Electric Vehicle (ICCEVE 2023). IET; c2023 Apr 12. p. 54-58.
12. Tripathi SL. Low-power high-performance tunnel FET with analysis for IoT applications. InHandbook of Research on the Internet of Things Applications in Robotics and Automation. IGI Global; c2020. p. 47-67.