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Zaid Siddiqui
Undergraduate Student, Electronics and Communication Engineering, SRM Institute of Science and Technology, Kattankulathur, Tamilnadu, India

Correspondence
Zaid Siddiqui
Undergraduate Student, Electronics and Communication Engineering, SRM Institute of Science and Technology, Kattankulathur, Tamilnadu, India

Review paper on low power VLSI design techniques

Zaid Siddiqui

Abstract
In the modern field of online industries, one of the most prominent trends that has evolved is a focus on using less power. In the design of VLSI chips, leakage current has risen to the level of importance formerly reserved for throughput and area. Because of the growing complexity, decreasing power usage and overall energy management on chips are the primary problems below 100 nanometers. This is because technology is shrinking. Because of the necessity to cut down on packaging costs and increase battery life, several designs place a significant emphasis on optimizing power consumption in addition to timing.
Inductance plays a crucial role with low wattage VLSI designs, not just for power usage and for power usage. The amount of power that is lost due to integration circuits' overall power loss is becoming more critical, with leakage current playing an increasingly significant role. This article provides an overview of the many power management methods, approaches, and techniques that may be used to low power circuitry. The future obstacles that should be overcome in order to create circuits with low power consumption and fantastic performance are indeed mentioned.

Keywords: Power dissipation, low power, process nodes, leakage current, power management

Introduction
The benefit of adopting a mix of low-power elements in tandem with approaches for limited design is much more valuable today than it has ever been in the past. As components are smaller, more useful, and powered by batteries at the same time, there is a continuing and considerable growth in the need for greatly reduced power usage. In the former, area, efficiency, and cost were the primary considerations for those who designed VLSI. The question of power is secondary to the primary priority. Today, power seems to be the prime concern despite notable growth and expansion in the profession of computer devices and cordless communication system, both of which request high speed arithmetic and complex features with low energy consumption. As a result, power consumption has become a primary concern. Different applications have different reasons for wanting to decrease their overall power usage. When it comes to the category of micro-powered lithium ion applications like mobile phones, the objective is to maintain a decent battery lifespan and weight while keeping costs of manufacturing as cheap as possible. The energy loss of the electrical components of a rising notebook computer, including a laptop, should ideally be reduced to a level that is approximately equivalent of both the system's overall power dissipation. This is the target. Last but not least, with high-performance, ou pas systems like workstations, the overarching purpose of necessary preventive is to cut down the expenses of the equipment while simultaneously assuring that the device will be reliable out over long run. Power consumption is becoming one of the most important factors to be considered of rising systems because of advancements in processing technologies. In technologies with process nodes smaller than 100 nanometers, power consumption owing to leakage now joined dynamic power as one of the key concerns for power usage. There are indeed a variety of strategies [15] which have been established over the course of the last decade to handle the continually aggressive wireless power transfer needs of the majority of rising systems. The fundamental approaches to low wattage design, like hardware implementation for the purpose of lowering switching activity and variable voltage sources (multi-Vt) again for purpose of lowering power dissipation, will be well and were supported through tools that are already on the market [17]. We are able to determine however many changes occur in circuitry by analyzing leakage power [15], which may be seen in Figure 1.

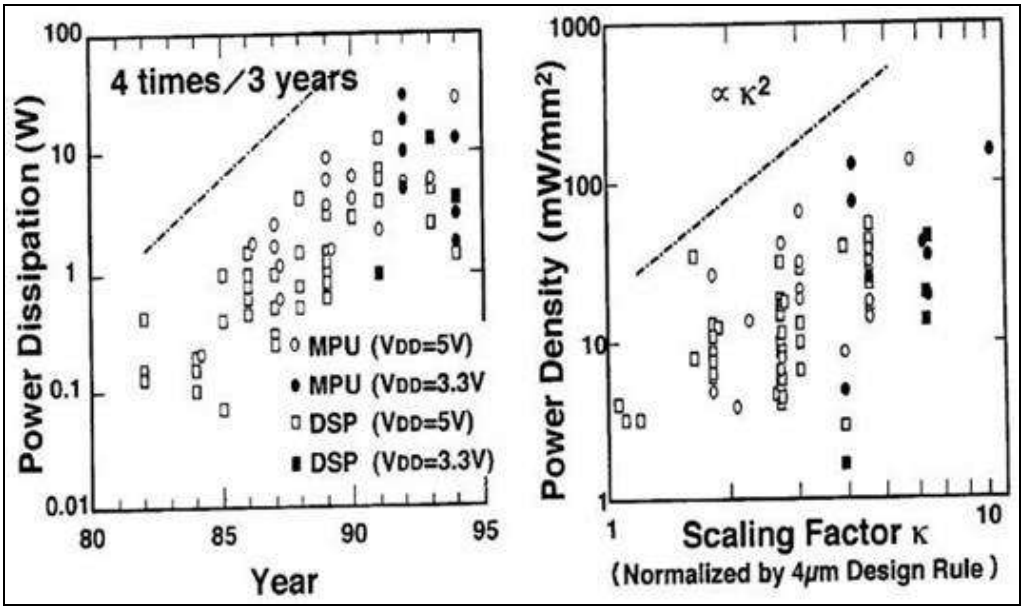

Fig 1: Evolution in power dissipation [15]

Low power strategies

Table I outlines the many approaches that may be used at various stages of the Cmos construction process in order to maximize efficiency in terms of power usage.

Table 1: Strategies for low power designs

Design Level	Strategies
Operating System Level	Portioning, Power down
Software level	Regularity, locality, concurrency
Architecture level	Pipelining, Redundancy, data encoding
Circuit/Logic level	Logic styles, transistor sizing and energy recovery
Technology Level	Threshold reduction, multi threshold devices

Power dissipation basics

The dissipation of power in such a circuit may be broken down into these three categories: dynamic energy, power lost due to short circuits, and based system. Out of some of the, load demand, also known as switching power, refers to the energy loss mostly during the process of charge/ discharge capacitors; its characteristics are outlined below [5, 6]:

$$P_{dynamic} = CL\ Vdd2\ \alpha\ f \quad (1)$$

Where CL denotes the load impedance, which is determined by the supporter, communication range, and transformer size; Vdd denotes the voltage source, that has been decreasing with each consecutive process node; denotes the exercise factor, which indicates how frequently, on ordinary, the coax cables switch; and f denotes the clock signal, that has been continuing to increase with each subsequent process node. This supply voltages (Vdd), variable switching cutoff (Vt), and the device sizes all have a role in determining the amount of operating voltage, also known as power losses (Figure2). Leaking becomes an increasingly form of energy usage as processes nodes diminish, and it consumes at most 30 percent of total electricity. Crowbar winds are another factor that contributes to the leaky energy dissipation [17]. These currents are created if both the Npn and Pnp devices are turned on at the same time. The vast majority of approaches for network level minimization primarily concentrate on minimizing comment thread leakage and do not take into account the consequences of gate leaking [15]. In order to lessen the amount of low current fault current that occurs during sleep mode, the MTCMOS technique described in has already been suggested. The many components that are responsible for such power loss in CMOS are shown in Figure 2.

Low power design space

The preceding section reveals that the Low power vlsi space has 3 functions: voltage, mechanical capacitance, & informational activity. These three variables are described in more detail below. In order to maximize available power, it is necessary to aim to minimize at least either of these parameters. In the following paragraphs, their significance in the procedure of power optimization will be discussed briefly.

Voltage

Reducing the voltage, which has a quadratic connection to power, is perhaps the most efficient way for cutting down on the amount of power that is used. A drop in voltage level by a series of 2 results in reduced in power usage by a four - fold, and this may be accomplished without the need of any specialized circuitry or technologies. Sadly, there seems to be a speed cost associated with reducing the voltage source, and delays dramatically rise as Vdd gets closer to the vth Vt of gadget. Changing the vth of the sensors is the strategy that may be used to lower the voltage source without resulting in a reduction in throughput. By lowering the Current source, the power supply may be decreased without

resulting in a decrease in performance. The need to provide suitable noise buffers and regulate the growth in the subthreshold fault current [6, 8, 10] establishes the limit for how lowest the Vt could go. This limit determines how low your Vt can just go.

Table 2: Low power techniques used today [1, 2]

Traditional Techniques	Dynamic Power Reduction	Leakage power reduction	Other Power reduction Techniques
Clock Gating	Clock Gating	Minimize usage of low Vt cells	Multi Oxide devices
Power Gating	Power Efficient Techniques	Power Gating	Minimize capacitance
Variable Frequency	Variable Frequency	Back Biasing	Power circuits
Variable Voltage Supply	Variable Voltage Supply	Reduce Oxide Thickness	
Variable Device Threshold	Variable Island	Use Fin FET	

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In the existence of varying corners, phases, and powered states, as well as production uncertainty [2, 3], design stage tools read the power purpose and accurately execute the layout. This includes the location of special units as well as routing and optimizing across power subdomains. Any use of various voltage islanders (domains) is becoming an increasingly frequent method for reducing power consumption in hardware layout. This method enables specific blocks to utilize supply voltages that are lower than most others, or being totally turned off, during certain modes. Shutters are a substantial contributor to the dynamic power consumption that occurs. In order to obtain significant power savings, low time tree synthesized (CTS) methodologies [5, 6] include reducing the capacitance of the whole circuit as well as the amount of switching frequency. However, able to get some best power findings from CTS is dependent on one's synthesize the oscillators for multiple nooks and modes simultaneously in the appearance of engineering and fabrication variability as well as in cross flows. This is necessary in order to achieve the best possible results. By briefly turning off the circuits, the voltage regulation approach is an excellent method for minimizing the amount of power lost due to leakage. This brief period of deactivation is also often referred to as "power saving mode" or "inactivated mode." If circuit components are needed for functioning again, they were activated into "active state," which means they are ready to perform their functions. The blocks may be turned off using either apps, depending on the user's preference. These days, a smart power controller that is devoted specifically to this task is often employed. The different power management strategies are compared with one another in Table 3, which details the related trade-offs.

Conclusion

The demand for systems with less power consumption is being pushed by a variety of market areas. Unfortunately, building for reduced wattage adds a whole new dimension to this already complicated design challenge, and the design must be improved not just for performance but also for electricity in addition to optimizing for area. By conclusion, the following are some of the most significant problems and concerns pertaining to small energy design features: -

1. Scalability of the Technology: It is related to various factors, including: the capacitive reactance per node decreases by 30 percent, the significantly raise in wiring base stations by 2 times, the uptick in die shape by 14 percent (in accordance with Logic circuits), the decrease in voltage level by 15 percent, and the higher incidence by 2 times. In order to address these concerns, the power output will be increased by a factor of 2.7.
2. Permeability power: In order to satisfy the demand for the desired frequency, Values will be raised, which also will result in a significant amount of power losses. A power supply of around 1V is the goal of this voltage

level / low threshold technologies and circuitry design philosophy. The thresholds at which the technology operates have also been lowered.
3. Methods of dynamic power usage, which include adjusting the voltage source and the pace at which operations are carried out in response to an assaying.
4. Low power connectivity, making use of advanced technologies, and an activities or swing reduction strategy.
5. The creation of power-aware methods, tools, and layouts for behavioral generation, logic formulation, and layout minimization.
6. Power-saving strategies that reuse the signal energy by exploiting the thermal switching concepts rather than dissipating these as heat. These techniques show promise in specific applications wherein speed may be traded for reduced power.

References

1. Michael Keating, David Flynn, Robert Aitken, Ala Gibsons and Kaijian Shi, Low Power Methodology Manual for System on Chip Design, Springer Publications, New York, 2007.
2. Creating Low-Power Digital Integrated Circuits The IZplementation Phase, Cadence, 2007.
3. Liu, Weidong, Xiaodong Jin, Xuemei Xi, James Chen, Min-Chie Jeng, *et al*. BSIM3v3.3 MOSFET Model User's Manual, Department of Electrical Engineering and Computer Sciences, University of California-Berkeley, 2005.
4. Glasser Lance A, Daniel Dobberpuhl W. The Design and Analysis of VLSI Circuits, Addison-Wesley Publishing Co, 1985.
5. Shekar Borkar. Design Challenges of Technology Scaling, IEEE Micro, 1999, pg 23.
6. Inukai T, *et al*. Boosted Gate MOS (BGMOS): Device/Circuit Cooperation Scheme to Achieve Leakage-Free Giga-Scale Integration, Proc. CICC, 2000, pp.409-412.
7. Hamzaoglu F, Stan M. Circuit-Level Techniques to Control Gate Leakage for sub 100nm CMOS, Proc. ISLPED, 2002, pp. 60-63.
8. Yeo Y, *et al*. Direct Tunneling Gate Leakage Current in Transistors with Ultrathin Silicon Nitride Gate Dielectric. IEEE Electron Devices Letters. 2000;21(11):540-542.
9. Mutoh S, *et al*. 1-V Power Supply High-Speed Digital Circuit Technology with Multi-Threshold Voltage CMOS. IEEE Journal of Solid State Circuits. 1995;30(8):847-854.
10. Alidina M, Monterio J, Devadas S, Ghosh A, Papaefthymiou M. Precomputation-based Sequential logic optimization for low power In Proceedings of the International Workshop on Low Power Design, 1994, 57-62.
11. Anand Iyer. Demystify power gating and stop leakage cold, Cadence Design Systems, Inc.
12. De-Shiuan Chiou, Shih-Hsin Chen, Chingwei Yeh. Timing driven power gating, Proceedings of the 43rd annual conference on Design automation, ACM Special Interest Group on Design Automation, 2006, pp.121-124.
13. Perman B. Design technologies for VLSI design, encyclopedia of computer science, 1995.
14. Mentor Graphics. Low power physical design with Olympus SOC, Place and route white paper, 2009.
15. Rahul Rao M, Jeffery Burns L, Richard Brown B. Circuit Techniques for gate and subthreshold leakage minimization in future CMOS technologies Proc. ISLPED, 2002, pp70-73.
16. Kao J, Siva Narendra, Ananta Chandra Kasan. Subthresh leakage modeling and reduction technique, 2002.
17. Prasad Subramanian. Power management for optimal power design, Esilicon, Corp, 2010.